CONTENT ADDRESSABLE MEMORY ARCHITECTURE PROVIDING IMPROVED SPEED

ABSTRACT OF THE DISCLOSURE

This invention provides, in an exemplary embodiment, a Content Addressable Memory ("CAM") architecture providing improved speed by performing mutually exclusive operations in first state of a clock cycle and by performing at least one operation, dependent on at least one previous operations, in the second state of the same clock cycles. The Content Addressable Memory (CAM) architecture comprises an array of CAM cells connected to a compare-data-write-driver and to a read/write block, for receiving the compare-data and for reading and/or writing data in the array of CAM cells respectively, outputs of the said CAM cell are coupled to a match block providing match outputs signal lines that identifies a match/no-match at the end of a search operation, and a control logic for implementing search and address decoding operations during first state and enabling read-or-write operations within the second state of the same clock cycle in the event of a match.